REMARKS

Related to the Claims

Claims 4 and 10 were amended. Claim 10 was amended to correct an informality. Claim 4 was amended to more clearly claim the disclosed circuit structures.

Reconsideration of the claims is respectfully requested.

Claim Rejections -- 35 U.S.C. § 102

Claims 1-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,177,839 to *Ishihara.*

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

In rejecting independent Claim 1 on page 3 of the July 25, 2003, Office Action, the Examiner identifies load resistors 15 and 16 of the *Ishihara* reference as a first and second load impedance, respectively, and asserts that transistors 11 and 12 show the claimed limitation "wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively." (emphasis added) The Applicants respectfully assert that the Examiner has mischaracterized the claim language. The language claims a first load impedance bridged to a predetermined part by at least one of the second output branches of the second differential amplifier stage and a second load impedance bridged to a

predetermined part by at least one of the second output branches of the third differential amplifier stage.

In contrast, the second output branch of the second differential amplifier stage of the *Ishihara* reference, the collector of transistor 11, is connected across both load resistors 15 and 16. Similarly, the collector of transistor 12, forming the second output branch of the third differential amplifier stage, is also connected across both load resistors 15 and 16. Thus, the *Ishihara* reference does not show a controllable amplifier arrangement "wherein the first and the second load impedance are bridged to a predetermined part by at least one of the second output branches of the second and third differential amplifier stages, respectively" as recited in Claim 1. As a result, *Ishihara* fails to anticipate the Applicants' invention as recited in Claim 1 (and Claims 2, 3 and 7-9 depending from Claim 1).

Independent claim 4 has been amended to more clearly claim the circuit structure of the Applicants' invention. As recited in the amended claim, a first load impedance is connected across the first and second output branches of the second differential amplifier stage and a second load impedance is connected across the first and second output branches of the third differential amplifier stage.

This may be contrasted with load impedances 15 and 16 of the *Ishihara* reference, which, together, are connected across the output branches of both the second and third amplifier stages. Nothing in *Ishihara* teaches or suggests the circuit structure as claimed in amended independent Claim 4. As a result, *Ishihara* fails to anticipate the Applicants' invention as recited in Claim 4 (and Claims 5, 6 and 10-16 depending from Claim 4).

Regarding independent Claim 17, the Examiner asserts that *Ishihara* shows "a first second-stage impedance load (15) coupled to the first second-stage output branch; a second second-stage impedance load (16) coupled to the first second-stage impedance load and to the second second-stage output branch (11), ... the first and second second-stage impedance loads for generating a first output voltage at output tap (18) coupled between them." (July 25, 2003, Office Action; page 7) The Applicants respectfully point out that, rather than being coupled between load resistors 15 and 16, output terminal 18 is actually coupled to the first output branch of the second-stage differential amplifier, along with load resistor 15.

The Examiner makes a similar assertion on page 8 of the July 25, 2003, Office Action that output terminal 19 shows an output tap between first and second third-stage impedance loads. Output terminal 19, too, is actually coupled to the first output branch of the third-stage differential amplifier, rather than being coupled between load resistors 15 and 16. Thus, *Ishihara* does not teach an output tap coupled between first and second impedance loads, as recited in independent Claim 17.

Furthermore, the Examiner has asserted that load resistor 15 of the *Ishihara* reference shows two elements of Claim 17, the "first second-stage impedance load" and the "second third-stage impedance load," and that that load resistor 16 shows two elements of Claim 17, the "second second-stage impedance load" and the "first third-stage impedance load." The Applicants respectfully assert that two elements in a prior art reference cannot teach four claimed elements. For all the above reasons, *Ishihara* fails to anticipate the Applicants' invention as recited in Claim 17 (and Claims 18-20 depending from Claim 17).

Therefore, the Applicants' respectfully assert that the rejection of Claims 1-20 under 35 U.S.C. § 102(e) has been overcome. Accordingly, the Applicants respectfully request withdrawal of the rejection and full allowance of Claims 1-20.

SUMMARY

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***wmunck@davismunck.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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